

may be output to a digital to analog converter (DAC) and LCD display engine or other suitable display device. In addition, such systems typically use separate data packers, one dedicated to each display engine, and only one of the packers includes a keyer. The second packer does not provide overlay information, and as such, simply packs the display data in a form that is understood by the DAC.

Please replace the paragraph beginning at page 6, line 6, with the following rewritten paragraph:

Each of the video overlay generators includes a graphics data unpacker 220a and 220b, a keyer 222a and 222b, and a data packer 224a and 224b. The unpackers 220a and 220b are operative to unpack packed graphics data 28a and 28b, received from respective display engines 24a and 24b. Each keyer 22a and 22b is operatively coupled to the graphics data unpackers 22a and 22b to receive unpacked graphics information 228a and 228b. Each of the keyers 22a and 22b is also responsive to selectively routed video data 18 from the programmable switching mechanism 16. As such, each keyer, 22a and 22b, suitably determines, based on the packed graphics information, the video window for which the selectively routed video data 18 is to be positioned within a display screen as known in the art. Data packers 24a and 24b received the keyed graphics and video information and pack the combined video and graphics information to generate the overlay information 30a and 30 b as known in the art.

Please replace the paragraph beginning at page 6, line 19, with the following rewritten paragraph:

The selectable video clock source 202 is coupled to the common video scaler 12 by providing the single video clock signal 38. The video scaler 12 scales input video 14 corresponding to a display engine 24a or 24b by providing scaled video to the programmable switch 16 which then switches the video to the appropriate video overlay generator 20a or 20b, depending upon the control signal 32. The common (e.g., single) video scaler includes line buffer 221 and video scaler 223. The video scaler 223 receives the video data from line buffer 221 and window timing control signal 225 while line buffer 221 receives the single video clock signal 38. The stored lines of video data are then scaled by the scaler 223 as known in the art. As such, the video scaler scales the video in response to the video clock signal output 38 such